

FIG.1

SURROUNDING LOGIC 46 20 42 LATCH LATCH 38 PATH P₁ PATH P_2 36 40 8 33 34 24 26 28 LATCH LATCH LATCH LATCH SURROUNDING LOGIC 48

FIG.2

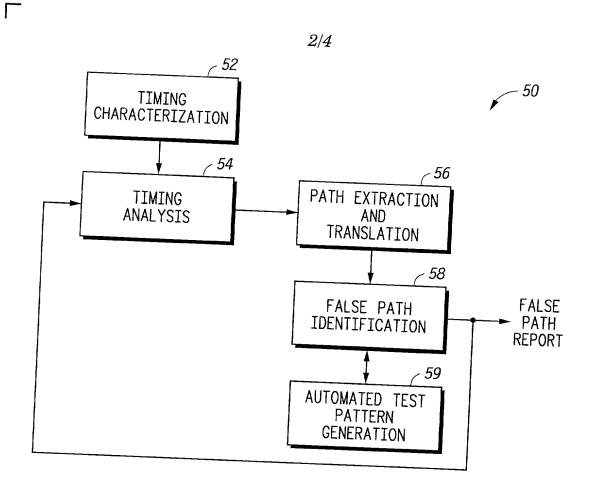


FIG.3

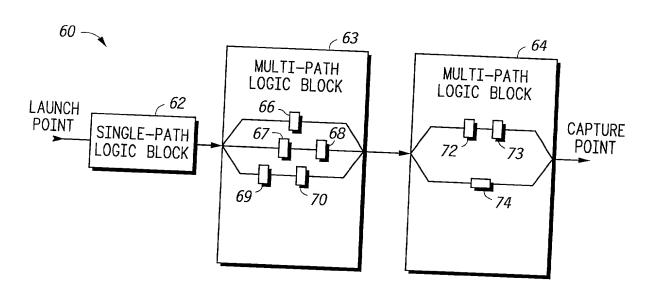


FIG.4

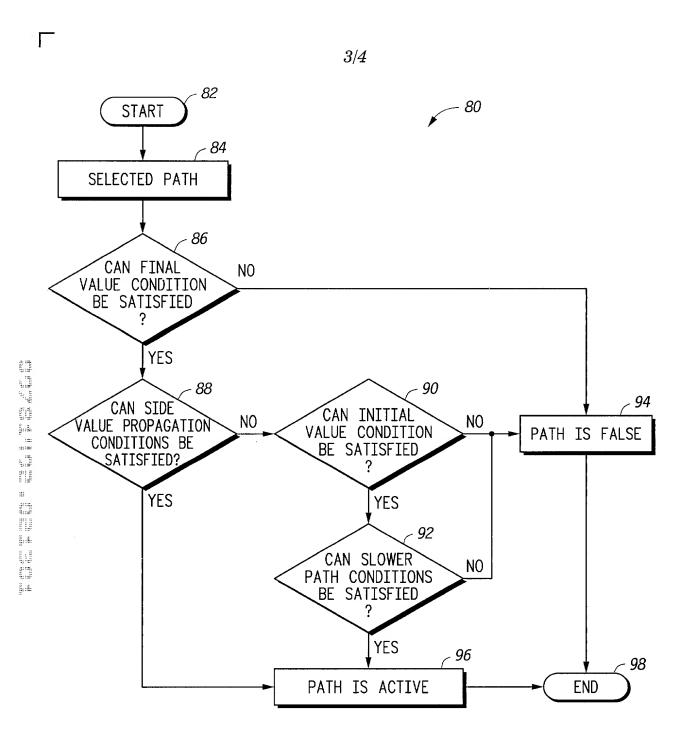


FIG.5

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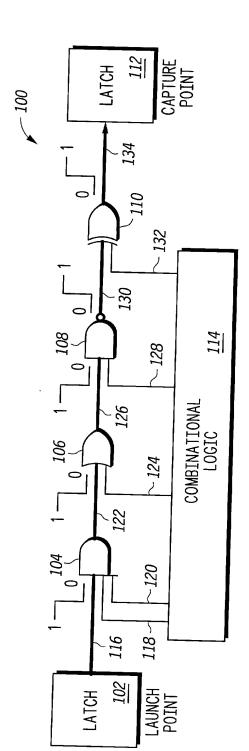


FIG.6

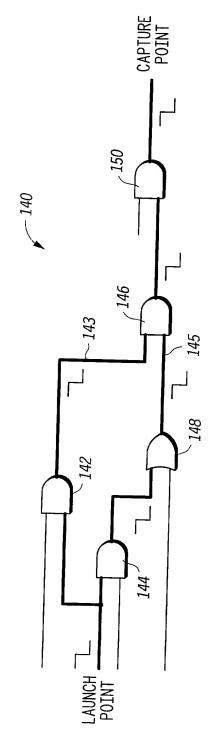


FIG. 7

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